REMARKS/ARGUMENTS

1. Amendments to the specification

The typographical error is corrected. No new matter is introduced. Consideration of the amendments is respectfully requested.

2. Amendments to the Claims

Claim 1 is amended to correct a grammatical error. In addition, the limitation "the output end of the npn Darlington circuit being grounded" is deleted without disclaimer.

Claim 13 is newly entered. As disclosed in specification paragraph [0023], the circuit 26 is complementary to the ESD protection circuit 10 in Fig. 3, and includes PNP BJTs and a PMOS transistor, where the circuit 26 is added between the source VDD and the input pad 22. Since the electrostatic current flows to the input pad 22 from the source VDD, an input end of the pnp Darlington circuit is connected to the source VDD, and an output end of the pnp Darlington circuit is connected to drain of the PMOS transistor. In addition, a control end of the pnp Darlington circuit is connected to the source of the PMOS transistor.

No new matter is introduced. Consideration of the amendments is respectfully requested.

3. Claim rejections – 35 U.S.C. 103(a)

Claims 1, 10, 11, and 12 were rejected under 35 U.S.C. 103(a) as being unpatentable over Nelson in view of Voldman et al. Claims 2-3 were rejected under 35 U.S.C. 103(a) as being unpatentable over Nelson in view of Voldman et al. and Glica and Williams et al. Claims 7-8 were rejected under 35 U.S.C. 103(a) as being unpatentable over Nelson in view of Voldman et al. and Li and Chen et al.

Response:

Claim 1

In this Office action, the Examiner stated that Nelson discloses an electrostatic discharge protection circuit comprising an NMOS transistor (Fig. 1 element 18), a drain of the NMOS transistor connected to the input end of the transistor circuit (Fig. 1 drain connected to V_{SS}), and a source of the NMOS transistor connected to a control end of the transistor circuit (Fig. 1 source connected to V_{DD}). However, applicants deem that the Examiner misinterprets Nelson's teachings.

Firstly, as known to those skilled in this art, V_{DD} represents a high voltage level and V_{SS} represents a low voltage level, i.e. the voltage level of V_{DD} is higher than that of V_{SS}. The transistor 18 shown in Nelson Fig. 1 is an NMOS transistor. Therefore, a drain of the transistor 18 should be coupled to V_{DD} instead of V_{SS}, and a source of the transistor 18 should be coupled to V_{SS} instead of V_{DD}. In addition, Nelson teaches "The condition pulls the control node 28 low, so that the voltage on the base of transistor 15 is biased so as to allow transistor 15 to conduct (col.1, line 66 to col. 2, line 1)." Therefore, the drain of the NMOS transistor 18 is connected to the control node 28, i.e. the base of the transistor 15. As a result, Nelson does not teach or suggest connecting the source of the NMOS transistor 18 to the control end 28.

Secondly, Nelson teaches using a voltage clamping PNP transistor 15 having its emitter and collector connected to V_{DD} and V_{SS}, respectively (col. 1, lines 42-43). Therefore, the transistor 15 is implemented by a pnp BJT. However, Voldman teaches using an npn Darlington circuit (Fig. 6) for electrostatic discharge protection. If the voltage clamping **PNP** transistor 15 (Nelson Fig.1) is replaced with the **NPN** Darlington circuit (Voldman Fig. 6), the protection circuit 10 disclosed by Nelson will be unable to operate correctly.

As taught by Nelson, the non-conduction of the control transistor 18 causes the control node 28 to remain at a high voltage level (col. 1, lines 56-58). Therefore, because a control end of the NPN Darlington circuit, disclosed by Voldman, is connected to the control end 28 shown in Nelson Fig. 1, the NPN Darlington circuit is enabled when the NMOS transistor 18 is turned off. Therefore, the normal operation of following circuit blocks is influenced by the abnormal activity of the ESD protection circuit. Similarly, when the NMOS transistor 18 is turned on due to electrostatic discharge, the low voltage at the control end 28 might disable the NPN Darlington circuit. Therefore, an ESD protection failure occurs.

As stated in MPEP 2143.01 "If proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification. In re Gordon, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984) it is stated "If the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims prima facie obvious. In re Ratti, 270 F.2d 810, 123 USPQ 349 (CCPA 1959), the combination of Nelson and Voldman's teachings is not proper. In short, it is not obvious to one having ordinary skill in the art at the time the invention was made to modify the Nelson device with the Voldman Darlington features.

In addition, as mentioned above, Nelson does not teach or suggest connecting the source of the NMOS transistor 18 to the control end 28. Even though the combination of Nelson and Voldman's teachings is reasonable, the claimed feature "a source of the NMOS transistor connected to a control end of the npn Darlington circuit" is neither taught nor suggested.

Applicants believe that claim 1 has been placed in condition for allowance. Consideration

of claim 1 is respectively requested.

Claims 2, 3, 7, 8, and 10-12

Since there is no suggestion or motivation to modify Nelson's device with Voldman's Darlington circuit, the claimed features in claims 10-12 are not anticipated by Nelson in view of Voldman, the claimed features in claims 2 & 3 are not anticipated by Nelson in view of Voldman, Glica and Williams, and the claimed features in claims 7 & 8 are not anticipated by Nelson in view of Voldman, Li and Chen. In short, claims 2, 3, 7, 8, and 10-12 are dependant upon claim 1, and should be allowed if claim 1 is found allowable. Consideration of claims 2, 3, 7, 8, and 10-12 is respectfully requested.

4. New claim

Claim 13 claims a complementary circuit of an electrostatic discharge protection circuit claimed in claim 1. Therefore, claim 13 should be found allowable if claim 1 is found allowable. Consideration of the newly entered claim 13 is respectfully requested.

Applicants respectfully request that a timely Notice of Allowance be issued in this case.

Sincerely yours,

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